DR. TANMAY DUBEY

ASSISTANT PROFESSOR
Electronics and Communication Engineering
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PROFESSIONAL EXPERIENCE:

- Assistant Professor at Indian Institute of Information Technology Surat from **September 2022 – to Present.**
- Assistant Professor in IET, Lucknow from **September 2021** to **July 2022.**
- Assistant Professor in Meerut Institute of Engineering and Technology, Meerut from **October 2020** to **August 2021.**

EDUCATION:

Ph.D. in Electronics and Communication Engineering from MNNIT Allahabad.

M.Tech in **VLSI Design** from **Thapar University, Patiala.**

B.Tech in **Electronics and Communication Engineering** from **Greater Noida Institute of Technology (GBTU), Greater Noida.**

RESEARCH INTEREST:

Analog circuit design, VLSI Design.

RESEARCH PUBLICATIONS:

SCI Journals:

[1] **Tanmay Dubey** and Vijaya Bhadauria, "A Low-Voltage Two-Stage Enhanced Gain Bulk-Driven Floating Gate OTA." *Journal of Circuits, Systems and Computers*, vol. 30, no. 12, 2150220 (2021).

[2] **Tanmay Dubey** and Vijaya Bhadauria, "Linearity Improvement of Bulk Driven Floating Gate OTA Using Cross-Bulk and Quasi-Bulk Techniques." *Journal of Circuits, Systems and Computers*, vol. 30, no. 07, 2150124 (2021).

[3] **Tanmay Dubey** and Vijaya Bhadauria, "A low-voltage highly linear OTA using bulk-driven floating gate MOSFETs," *AEU - Int. J. Electron. Commun.*, vol. 98, pp. 29–37, 2019.

[4] **Tanmay Dubey**, Vijaya Bhadauria and Rishikesh Pandey, "Linearity Enhancement Techniques for Operational Transconductance Amplifier: A Survey", Recent Advances in Electrical & Electronic Engineering (2020) 13: 5, pp. 650 - 668 https://doi.org/10.2174/2352096512666191019130214

[5] **Tanmay Dubey** and Rishikesh Pandey, "Low-Voltage Highly Linear Floating Gate MOSFET Based Source Degenerated OTA and its Applications," *Inf. MIDEM*, vol. 48, no. 1, pp. 19–28, 2018.

[6] Nikhil Deo, Tripurari Sharan and **Tanmay Dubey**, "Subthreshold biased gain enhanced bulk-driven double recycling current mirror OTA," *Analog Integrated Circuit and Signal Processing*, vol. 105, no. 2, pp. 229-242, 2020.

International Journals:

[7] **Tanmay Dubey**, Rishikesh Pandey and Sanjay Sharma, "Highly Linear Source Degenerated OTA Using Floating Gate MOSFET Technique," *VLSI Circuits Syst. Lett.*, vol. 4, no. 2, pp. 2–7, 2018.

Book Chapters:

[8] **Tanmay Dubey** and Vijaya Bhadauria "A Linear OTA using Series Connected Source Degenerated Bulk Driven Floating Gate Differential Pairs," *2019 2nd Int. Conf. VLSI, Communication and Signal Processing, VCAS 2019.*

[9] **Tanmay Dubey**, Ravishankar and Vijaya Bhadauria, "Cross Coupled Bulk Degenerated OTA using Source Follower Auxiliary Pair to Improve Linearity," *2018 1st Int. Conf. VLSI, Communication and Signal Processing, VCAS 2018,* Springer.

[10] **Tanmay Dubey**, Anurag Kumar and Vijaya Bhadauria, "Highly Linear Source Degenerated OTA with Floating Gate Auxiliary Differential Pair," *2018 1st Int. Conf. VLSI, Communication and Signal Processing, VCAS 2018,* Springer.

International Conferences:

[11] Utkarsh Sharma, **Tanmay Dubey** and Vijaya Bhadauria, "Linearity Enhancement using Bulk-Degeneration for Source Degenerated OTAs," *2018 2nd Int. Conf. Advances in Electronics, Computer and Communications, ICAECC-2018.*

[12] Shanu Kumar, Vijaya Bhadauria, and **Tanmay Dubey**, "LVLP high gm bulk-driven folded cascode OTA using current shunt auxiliary pair," *2017 4th Int. Conf. Power, Control Embed. Syst. ICPCES 2017*, vol. 2017–January, no. 1, pp. 1–5, 2017.

ACHIEVEMENTS:

- Reviewer of several peer-reviewed international journals.
- GATE qualified in the year 2011, 2012, 2015 and 2020.
- Ph.D. institute scholarship.
- UGC NET 2015 qualified for Assistant Professor.
- Silver medalist in 51th Annual Sport Meet 2018 in MNNIT Allahabad.